Abstracts

SiO/sub 2/ interface layer effects on microwave loss of high-resistivity CPW line

Yunhong Wu, S. Gamble, B.M. Armstrong, V.F. Fusco and J.A.C. Stewart. "SiO/sub 2/ interface layer effects on microwave loss of high-resistivity CPW line." 1999 Microwave and Guided Wave Letters 9.1 (Jan. 1999 [MGWL]): 10-12.

For a coplanar waveguide (CPW) line where the metal conductor is in direct contact with the HR-Si substrate, the microwave losses are low but are sensitive to DC bias due to DC leakage current. With a continuous SiO/sub 2/ layer inserted between the CPW metallization and HR-Si substrate, DC leakage is eliminated, but microwave losses increase. An MOS C-V analysis shows that an induced charge layer exists on the substrate surface and is the principle cause for increased line losses. If the insulated SiO/sub 2/ layer beneath the conductor strips of line is made to be noncontinuous, then microwave losses are decreased from 18 to 3 dB/cm at 30 GHz.

❑ Return to main document.